ASE GROUP
A SUCCESS ENABLER

ASE news

ASE Advances in Fine Pitch Wire Bonding Technology

Patented tri-tier wire bonding technique successfully developed to enable semiconductor chips with smaller area and denser I/Os.

Santa Clara, California, July 25th, 2002 – Advanced Semiconductor Engineering Incorporated (ASE) (TAIEX: 2311, NYSE: ASX), one of the world's largest semiconductor packaging and testing companies, unveils today its tri-tier fine pitch (FP) wire bonding development. In tri-tier FP wire bonding, three rows of wiring protrude from the IC pads to provide connectivity to other parts of the IC package. The inner, middle and outer wires are isolated by different loop heights to prevent wire shorting.

Earlier generations of FP wire bonding techniques utilizes in-line pad pitch (single rows of wire) and subsequently staggered pad pitch (two rows of wire) in IC packages. However, as ICs become more complex in design and the demands for its performance increases as the die size decreases, in-line and staggered wire bonding had shortcomings. The increased density of pads and the limited capability of existing packaging equipment and materials caused the lack of intensity in the wire interconnections, which often resulted in lower reliability and frustrated the development of high I/O chip designs. ASE began research into more advanced wire bonding techniques and with the availability of advanced wire bonding equipment, developed the tri-tier FP wire bonding technology to address these challenges. ASE's tri-tier wire bonding technology is suitably applied to ICs that require the integration of multiple functions onto a limited area such as the chipsets within PCMCIA and multimedia/graphics cards in desktop and notebook PCs.

ASE currently offers its tri-tier FP wire bonding process in plastic ball grid array (PBGA) of as low as 70um and will offer down to 60um at the end of 2002. ASE's tri-tier wire bonding technology received U.S. and Taiwan patents in 2001. "With IC designers placing more circuits within a smaller die area, and pushing the limits of chip performance, related packaging techniques will need to be improved," said J.J. Lee, Vice President of Research and Development, ASE Group. "In addition to our fine pitch wire bonding, we have also developed two to three layers of pads designed to enable chip miniaturization. ASE's packaging techniques will certainly contribute to the

growth in design and development of hi-tech electronic products yielding higher quality and lower cost," he added.

About ASE Inc.

ASE Inc. (TAIEX: 2311, NYSE: ASX) is one of the world's largest independent providers of semiconductor packaging services and, together with its subsidiary ASE Test Limited (Nasdaq:ASTSF), the world's largest independent providers of semiconductor testing services, including front-end engineering testing, wafer probing and final testing services. The Company's international customer base of more than 200 blue-chip customers includes such leading names as Advanced Micro Devices, Inc., Altera Corporation, Cirrus Logic Inc., Conexant Systems, Inc., LSI Logic Corporation, and Qualcomm Inc. With advanced process technology capabilities and a global presence spanning Taiwan, Korea, Singapore, Malaysia and the United States, ASE Inc. has established a reputation for reliable, high quality products and services. For more information, visit the website www.aseglobal.com

###

Contact Information:

Clementine Chen / Freda Wan
ASE Asia Pacific
+886-2-8780 5489
clementine_chen@aseglobal.com
teri_chen@aseglobal.com

Jennifer Yuen / Charles Chiu
ASE Americas/Europe
+1-408-9866519 / +43-664-141 1201
jennifer.yuen@aseus.com
charles.chiu@aseeu.com