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ASE news

ASE completes internal development of electroplated wafer bumping technology

- *Electroplating process enables finer bump pitch capabilities to meet package requirements for high end computing and networking products*
- *Technology fully researched and developed internally*
- *First semiconductor packaging company to offer customers choice of bumping methods including printing and electroplating inhouse*

TAIPEI, Taiwan, April 9, 2003 - Advanced Semiconductor Engineering Incorporated (ASE, TAIEX: 2311, NYSE: ASX), one of the world's largest semiconductor packaging and testing companies, announced that its team of R&D engineers has successfully completed its internal development of electroplated wafer bumping technology on 200mm wafers and has begun a pilot run at its Kaohsiung manufacturing facility.

Wafer bumping has gained popularity due to the advent of the flip chip packaging technology that enables high performance for high density semiconductor chips. Electroplated wafer bumping offers many advantages for high pin count and fine pitch advanced packages that are widely applied in high end, high performance computing and networking products such as CPUs, PLDs, graphic chipsets and power ICs. ASE's electroplated process offers bumping capabilities of up to 3000 bumps per die. Reliability and performance of the dies are also improved significantly through the high lead process in electroplated wafer bumping.

In the initial phase of volume production, ASE is setting a monthly capacity of 10,000 pieces of 200mm electroplated bumped wafers. The company is currently the only semiconductor packaging service provider able to offer customers an integrated semiconductor packaging solution incorporating this technology within its own manufacturing facilities, i.e. from the delivery of wafers to ASE, to the probing, bumping, packaging, final testing and drop shipment to the customer.

"According to TechSearch International Inc, a packaging consultancy based in Austin, Texas, bumped wafers using the electroplated process is forecast to reach a capacity of 6,410,000 200mm-equivalent wafers this year, and will increase two-fold in the year 2005 to 12,688,000," said J.J. Lee, Vice President, Research and Development, ASE Group. "Demand for electroplated wafer bumping will continue to rise largely due to the increased application of flip chip packaging

technology whereby wafer bumping is an essential process. ASE analyses market trends closely and develops its technologies and resources in anticipation of customers' sophisticated chip designs and requirements."

ASE's wafer bumping technology developments began in 1999, and the company offers bumping services for 150mm, 200mm and 300mm wafers (current 300mm wafers in printed bumping technology) adding value to customers on top of its turnkey offerings in semiconductor backend services. With the gradual migration of the industry to 300mm wafers, ASE is also rapidly developing electroplated wafer bumping process to handle these larger wafers.

About ASE Group

The ASE Group is one of the world's largest providers of semiconductor manufacturing services. As a global leader geared towards meeting the industry's ever growing needs for faster, smaller and higher performance chips, the Group develops and offers a wide portfolio of technology and solutions including IC test program design, front-end engineering test, wafer probe, wafer bump, substrate design and supply, wafer level package, flip chip, system-in-package, final test and electronic manufacturing services through Universal Scientific Industrial Co Ltd, a member of the ASE Group. The Group generated sales revenues of \$2.33 billion in 2002 and employs 24,000 people worldwide. For more information about the ASE Group, visit <http://www.aseglobal.com>

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