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ASE news

ASE qualifies wire-bond and flip-chip assemblies for ICs using TSMC's all-copper, 0.13-micron low-K dielectric process technology

Results demonstrate successful implementation of company's package technologies with industry-leading chip manufacturing process.

TAIPEI, Taiwan, April 16th, 2003 - Advanced Semiconductor Engineering Incorporated (ASE, TAIEX: 2311, NYSE: ASX), one of the world's largest semiconductor packaging and testing companies, announced that it has worked closely with Taiwan Semiconductor Manufacturing Company (TSMC, NYSE: TSM) to successfully qualify ASE's wire bond BGA and flip chip BGA for use with TSMC's all-copper, 0.13-micron low-k ($k=2.9$) dielectric process technology.

The important functions of chip performance are high speed and low power consumption. The lower the dielectric constant (k) of the insulating medium of chip wires, the faster the electrical signal speed and the lower the power consumption. Replacing chip wires traditionally coated with silicon dioxide, with a lower k dielectric medium allows electronic signals to move faster through the chip interconnections. Coupled with the lower resistance properties of copper interconnects, low- k dielectrics provide significant improvement in overall IC performance.

However, low- k dielectric materials are of lower modulus and strength than silicon dioxide, presenting challenges at the packaging level. ASE has met those challenges, demonstrating outstanding reliability over thousands of hours of testing. Using a rigorous quality and reliability testing methodology, ASE has qualified its high performance wire bond and flip chip BGA packages with body sizes up to 37.5mm by 37.5mm.

"The accomplishment marks a significant milestone for ASE, as the industry in general has reported difficulties qualifying packages on low-K. ASE has gained a breakthrough after extensive research and development effort with TSMC, using new and advanced techniques," said Dr. Ho-Ming Tong, vice president of Advanced Technologies, ASE Group. "The use of flip chip packaging further enhances the performance of the copper low-K chip as the I/O pads are distributed all over the surface of the chip, allowing optimization of the circuit path and reduction of signal inductance."

"TSMC is already the foundry industry leader in the deployment of 0.13-micron manufacturing technology. By offering a process using low-k dielectrics, we provide our customers with the opportunity to substantially increase performance while reducing power," said Genda Hu, vice president of marketing at TSMC. "By qualifying wire bond and flip chip packaging schemes for this process, we can deliver an integrated solution, from chip to component, for our customers who want to gain the extra speed and power performance using the low-K dielectric process."

"TSMC is undoubtedly the leading foundry provider in the application of copper low-K dielectric materials on 200mm and 300mm wafers. Chips manufactured using this process technology are expected to quickly ramp in volume production due to their marked improvements in chip performance, increased speed and reduced power consumption," said J.J. Lee, vice president, ASE Group Research and Development. "As a leading manufacturing service provider, we continuously keep up with the technologies of our customers and partners in order to complement our packaging and testing services for next generation chips."

Meanwhile, ASE's R&D team continues to work on a wide portfolio of packages including flip chip and wire bond, on TSMC's 200mm and 300mm wafers. In addition, ASE is working on the qualification of its internal bumping capabilities on 300mm copper low-K wafers. Reliability data is available upon request. For more information, please contact your nearest ASE sales office or email marketing@aseus.com.

About ASE Group

The ASE Group is one of the world's largest providers of semiconductor manufacturing services. As a global leader geared towards meeting the industry's ever growing needs for faster, smaller and higher performance chips, the Group develops and offers a wide portfolio of technology and solutions including IC test program design, front-end engineering test, wafer probe, wafer bump, substrate design and supply, wafer level package, flip chip, system-in-package, final test and electronic manufacturing services through Universal Scientific Industrial Co Ltd, a member of the ASE Group. The Group generated sales revenues of \$2.33 billion in 2002 and employs 24,000 people worldwide. For more information about the ASE Group, visit

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